LAIKIPIA UNIVERSITY

UNIVERSITY EXAMINATIONS

1ST SEMESTER 2022/2023 ACADEMIC YEAR

SECOND YEAR EXAMINATION FOR THE DEGREE BACHELOR OF SCIENCE (COMPUTER SCIENCE)

COMP 213: COMPUTER ORGANIZATION AND ARCHITECTURE

STREAM: R ***TIME: 2 HRS***

DAY: WED [2.30PM – 4.30PM] ***DATE: 07/12/2022***

THIS QUESTION PAPER CONSISTS OF THREE (3) PAGES

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INSTRUCTIONS: -Answer Question 1 and any other two questions in the answer booklet provided.

QUESTION ONE

(a) Define the following terms (3 marks)
- (i) program?
- (ii) Machine Cycle
- (iii) Cache Memory

(b) Explain THREE factors that may make an organization adopt the use of off-shelf software (3 marks)

(c) Describe FIVE factors that may cause an organization to adapt the use of Information Communication Technology (5 marks)

(d) Explain FIVE symptoms of a faulty power supply unit (5 marks)

(e) Describe the four phases included in the main operations of the CPU (4 marks)

(f) Explain the different types of buses used to connect the different internal components of the computer system for the purpose of transferring data as well as addresses (4 marks)

(g) Explain different types of data manipulation instructions with examples (3 marks)

(h) Explain major characteristics of memory (3 marks)

QUESTION TWO

(a) Discuss the two major categories of the internal communication of a processor in the computer system (4 marks)

(b) Explain ways in which Control units can be implemented (4 marks)

(c) "RISC has the ability to use efficient instruction pipeline". Justify the statement. (6 marks)

(d) differentiate between computer architecture and computer organization. (6 marks)

QUESTION THREE

(a) Describe the functions of a computer. (4 marks)

(b) Outline the step involved in an interrupt cycle Interrupt Cycle. (4 marks)

(c) Explain different types of interconnections indeed required in Computer Architecture.

(d) Explain the characteristics of multiprocessors. (6 marks)

(e) Justify why priority interrupt is needed for data transmission between CPU and I/O device. (6 marks)

QUESTION FOUR

(a) Using a diagram showing the structure of the control unit (6 marks)

(b) What is the function of the following Expansion Buses / "slots" on the motherboard (4 marks)?

(i) ISA – Industry Standard Architecture
(ii) PCI – Peripheral Component Interconnect
(iii) EISA – Extended ISA
(iv) SIMM – Single Inline Memory Module

(c) Write an algorithm that implements a fetch sequence cycle (5 marks)

(d) Discuss problem associate with hard-wired designs (5 marks)

QUESTION FIVE

(a) Explain the steps involved in Instruction processing (5 marks)

(b) What are the problems associated with Single Bus Problems? (5 marks)

(c) Explain the interconnection with 'CPU with Memory and i/o devices along with different operations over them (5 marks)

(d) Why is micro-programmed control unit more flexible as compared to hardwired control unit? (5 marks)